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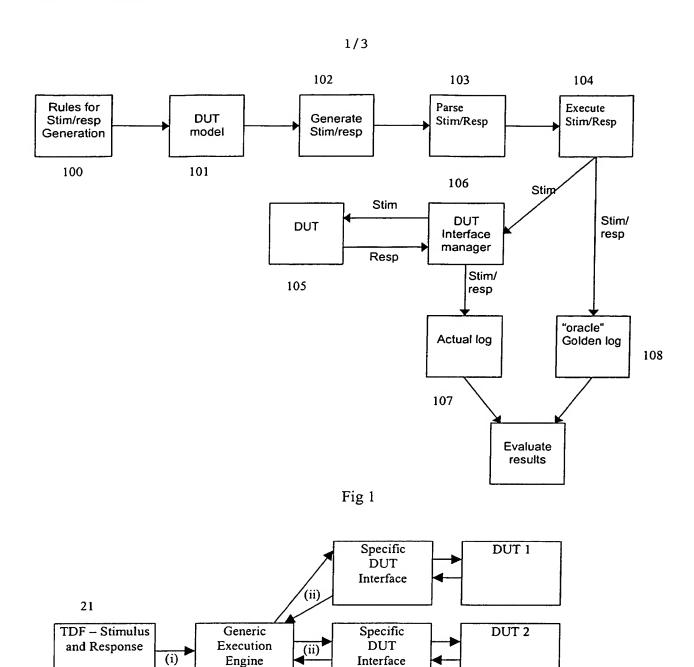


Figure 2Generic Execution Engine Architecture

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20

(iii)

Results Log

22

Specific

DUT

Interface

23

DUT N

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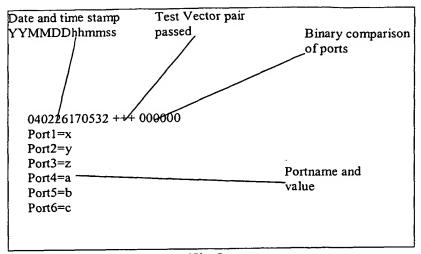


Fig 3a

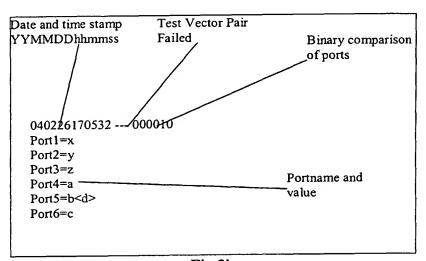
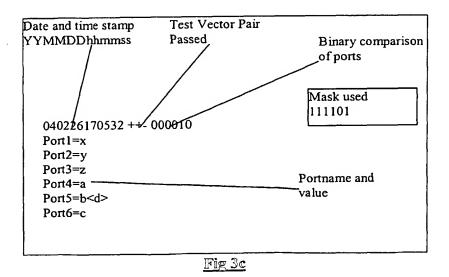


Fig 3b



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Input Port1	Input Port2	Input Port3	output Port4	Output Port5	Output Port6
X <sub>1</sub>	У1	$Z_1$	a <sub>1</sub>	b <sub>1</sub>	C <sub>1</sub>
X <sub>2</sub>	У2	$Z_2$	$a_2$	b <sub>2</sub>	C <sub>2</sub>
X <sub>3</sub>	Уз	$Z_3$	$a_3$	b <sub>3</sub>	C <sub>3</sub>
Xn	Уn	Zn	an	bn	Cn

Fig 4